cahiers techniques 2

protection of electrical distribution networks by the logic selectivity system

Roland Calvas
François Sautriau

MERLIN GERIN
service information
38050 Grenoble cedex
France
tél. (76) 57.60.60

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Summary
After a brief review of the conventional processes for selective tripping (overcurrent and time lag), the principle of the Logic Selectivity System (patented by Merlin Gerin) is described.
The Logic Selectivity relays Vigirack, mounted in Vigirack type 4 racks, are then presented ; they benefit from the experience which has been acquired since the commercialisation of the SSL relays in 1969.
A description of certain of their applications to the most conventional types of distribution networks is given, illustrating the advantages of this protection system.

introduction

If a fault occurs at any point in an electrical distribution circuit, it is essential that it does not interrupt the supply to all the workshops or offices of that network. This obvious requirement leads to the necessity of rapidly isolating the defective section without depriving the other users of electrical energy; this is in fact the principle of selective tripping.
The protecting element (circuit-breaker or fuses) which is placed immediately up-stream from the part of the circuit where the fault has occurred, and this alone element, must then operate; the other protecting elements must not trip.
Conventional selectivity processes (overcurrent and time lag) fulfil these requirements to a more or less satisfactory degree.
The Logic Selectivity System (Merlin Gerin patent) makes it possible to attain a total selectivity between all stages of an electrical distribution network from high to low voltages. It also allows the fault to be eliminated very rapidly and independent of the place where the fault occurred.

conventional selectivity processes and their limitations (1)

overcurrent selectivity

This makes use of protective equipment operating instantaneously (rapid circuit-breakers or fuses).
The selectivity is based on the fact that the short-circuit current decreases with increasing distance from the source. It is thus used especially for low voltages where the connecting impedances are not negligible.
If Ir is the current setting for instantaneous tripping and Icc is the short-circuit current which is established at the point of departure B, down-stream from the protection equipment,
selectivity is total
if Ir of A > Icc at B.
selectivity is partial
if Ir of A < Icc at B.

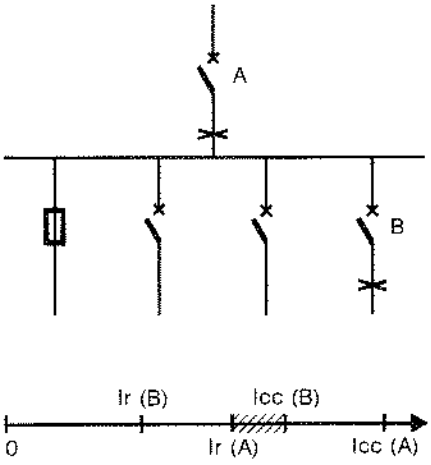


Figure 1

In fact, for any fault current occurring at the point of departure B, and having a value between Ir (A) and Icc (B), the two circuit-breakers A and B will open. Thus overcurrent selectivity, more or less partial according to the position of the fault, only rarely guarantees a selective tripping. Its main advantage is its low cost which justifies its use in simple installations.

time lag selectivity

This can provide complete selectivity by delaying the tripping of each circuit-breaker for durations all the higher as the circuit-breaker is nearer the source of energy.
In the example of Figure 2, the circuit-breakers D_1 are not delayed ; circuit-breakers D_2 are delayed for 0.3 sec, D_3 for 0.6 sec, and D_4 for 0.9 sec.
An unwanted consequence of these variable delays is that a fault in A will only be eliminated by D_4 in 0.9 sec. Furthermore, the time for eliminating the fault becomes too long when it occurs close to the source, and an incompatibility can arise between the selectivity and the shorter delay (0.2 sec at 20 kV) which the distributor allows for the supply circuit breaker.
These excessive delays have the disadvantage of necessitating a thermal over-sizing of the cables and especially of increasing considerably the dangers of damage due to arc propagation from the point of the fault.

logic selectivity

As we have just seen, overcurrent and timed selectivities have their weak points. Electricians have learnt how to live with them, often at the expense of the selectivity itself.
The Logic Selectivity System has been developed with the aim of correcting these disadvantages; it makes it possible to obtain a perfect tripping selectivity, and also to reduce considerably the delay in tripping the circuit-breakers closest to the source.

(1) see bibliography.

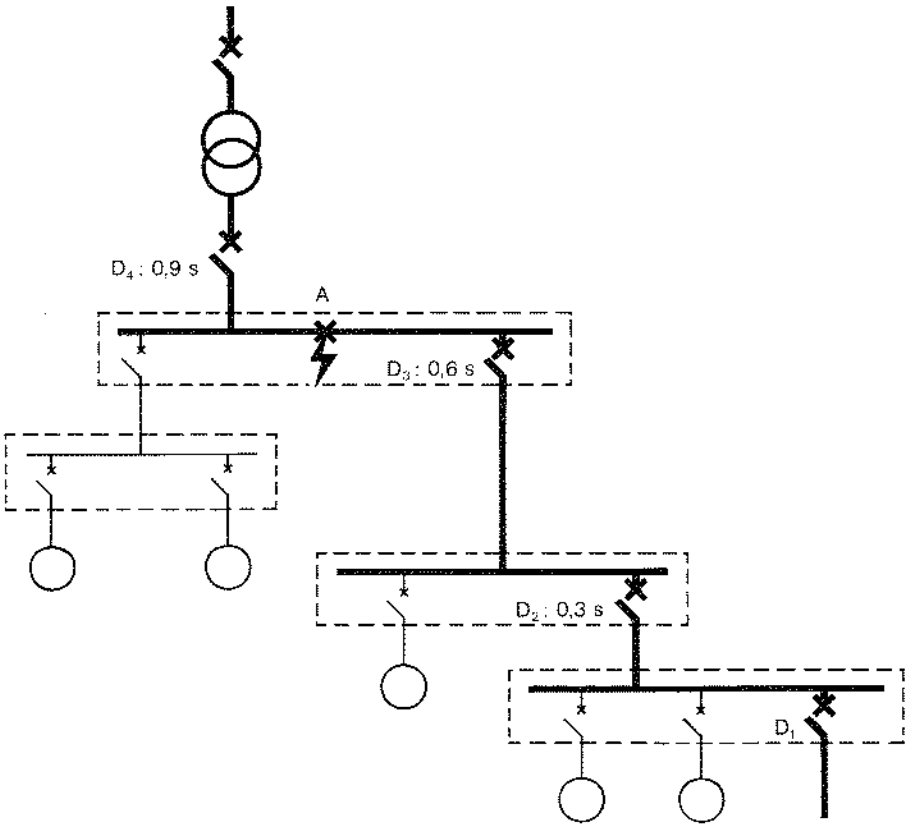


Figure 2

the principle of the logic selectivity system (SSL)[2]

Let us take the example of a radial distribution (Figure 3). For simplification, only a single departure point per stage is considered.

To each circuit-breaker is associated a "logic relay" (CAHL) receiving fault information from its detectors (C.T. rings) and emitting tripping and logic wait signals.

Any relay affected by a fault will send:

- a logic wait signal (LWS) to the up-stream stage (an order to increase the up-stream relay's own time-lag).
- a tripping signal to the circuit-breaker to which it is associated, unless it has itself received a logic wait signal from the down-stream stage.

In the example shown in Figure 3, **when a fault appears in A**, the (n) relays are each informed of this fault. The logic relay 1 sends a signal LWS to logic relay 2, and a tripping signal to the circuit-breaker D 1. The relay CAHL 2 places logic relay 3 momentarily in a waiting position, etc., the (n-1) CAHL transmitting a signal LWS to logic relay (n), right up to the supply source unless that, beyond a certain point, the fault current becomes lower than the thresholds settings (overcurrent selectivity).

The circuit-breaker D_1 opens after a time

$TD_1 = T_1^1 + t_1$

T_1^1 is the logic relay 1's own delay period

t_1 is the circuit-breaker D_1's own opening time (including the time of the arc).

If the fault appears in B, the CAHL 1 and D 1 are not affected and CAHL 2 does not receive the signal AL, then the fault will be eliminated in a time

$TD_2 = T_2^1 + t_2$

The same reasoning can be applied to any of the circuit-breakers in a distribution network.

The fault at stage "n" will be eliminated in a time

$TD_n = T_n^1 + t_n$

(2) see bibliography.

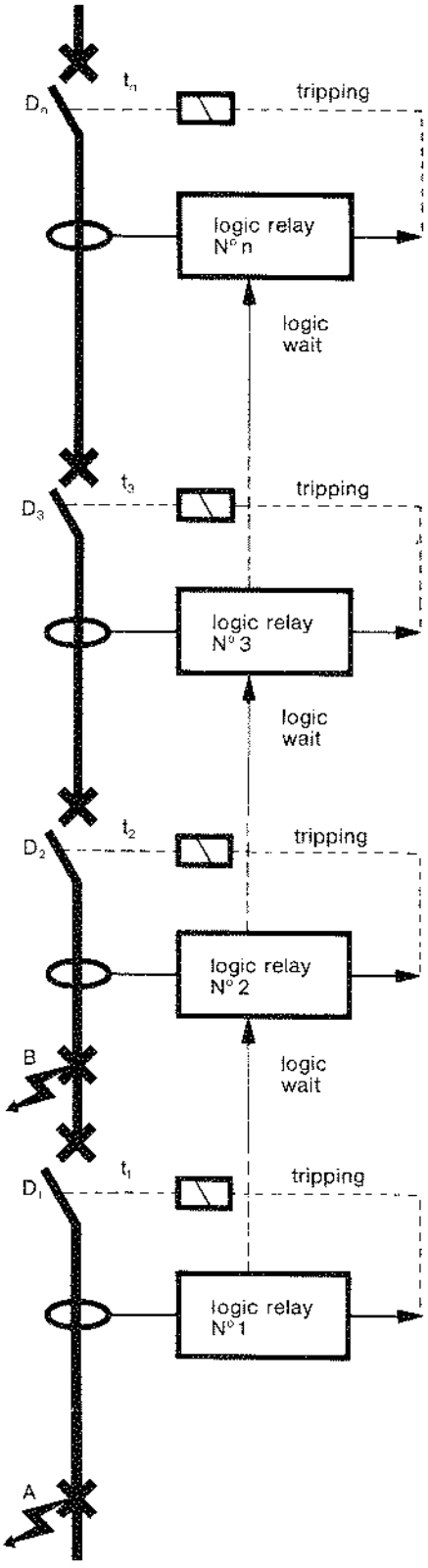


Figure 3

It can thus be seen that, with the Logic Selectivity System, the time necessary for eliminating faults can be very short, and especially as this time is independent of the number of stages; even better, generally speaking, the further one goes from the receivers, the shorter the time-lag T^1 is; this means that TD_n is often less than TD_1.

Remarks concerning the Logic wait function (see figs 4 and 5).

The wait time is not a locking operation, it is an increase Δt in the time-lag (T^1) of the up-stream relay. It comes into play as soon as the fault appears and only lasts as long as is necessary for the circuit-breaker of the stage considered to eliminate the fault, i.e.

$\Delta t = T^1 + t + \epsilon = T^1 + T^3$

The wait can in no case last too long, nor permanently block the up-stream relay; the reasons for this are:

- the presence of T^3 (having the function of suppressing the time-lag).
- the wait signal ceases if T_3 fails, thanks to the function T^2 (a limited delay function),
- in the case of a power cut or of a short-circuit, or of the earthing of the "pilot conductor", all delay times (Δt) are reduced to zero. In this case, the selectivity between the two stages disappears, but selective protection is still assured over the rest of the installation.

The vigirack type 4 rack[3]

(overcurrent, zero phase sequence logic)

This is a rack for indirect relays designed to protect high, medium and low voltage, 50/60 Hz circuits against the following faults:

- current surges (short-circuits)
- earth faults (appearence of a zero phase-sequence current). The modular design of this relay (a rack with plug-in relay PCB'S) makes it possible to obtain several variants:*

With overcurrent and logic PCB'S which does not possess the zero phase-sequence function, so its use is mainly reserved for networks with an isolated neutral.

(3) see bibliography
* see leaflet E/F 11-015 a

Schematic of the Vigirack type 4 rack

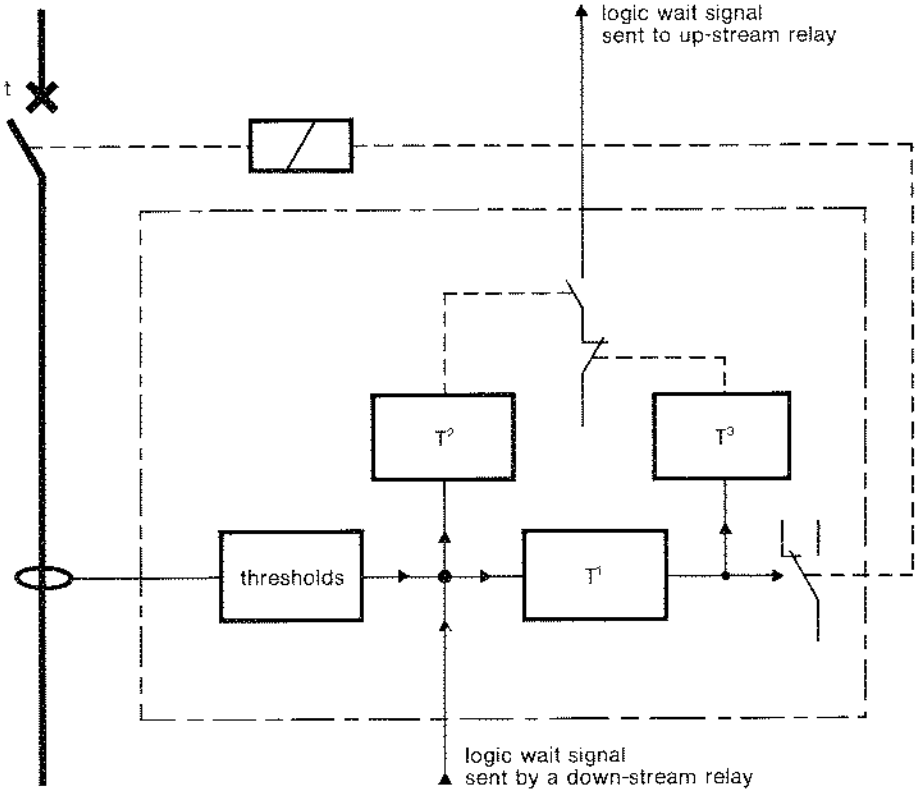


Figure 4

Graphical representation of intervention of different time relay.

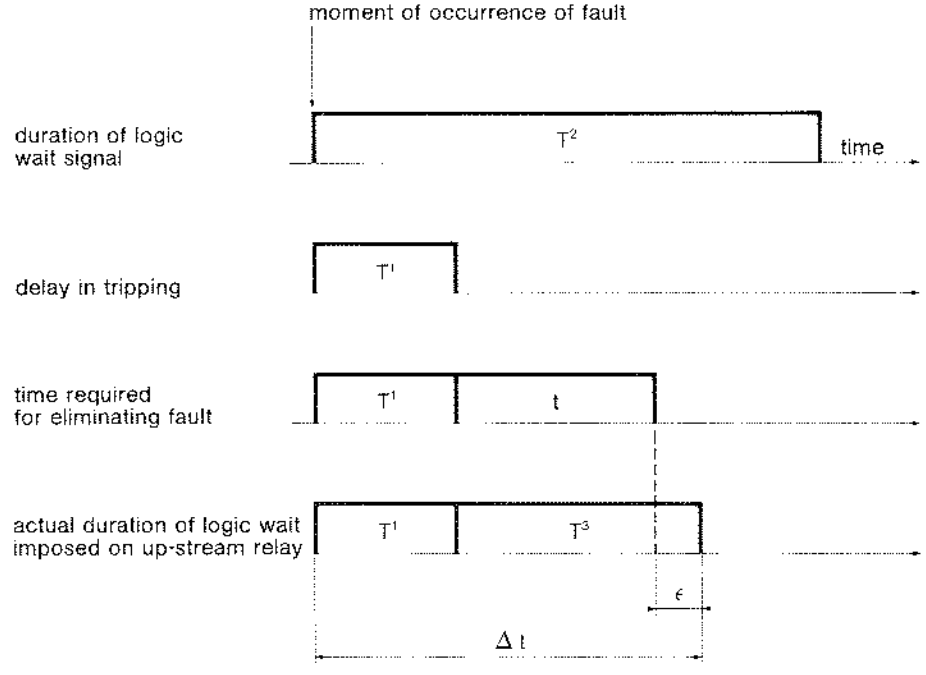


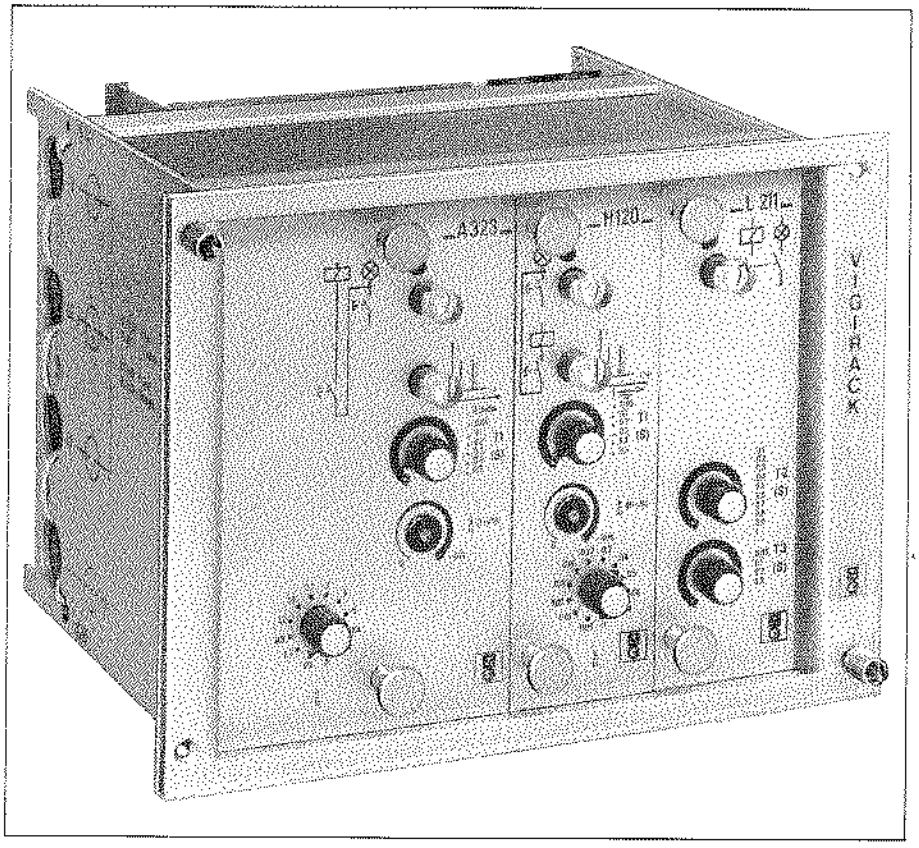
Figure 5

With zero phase-sequence and logic PCB'S
which does not possess the overcurrent function so its most commun application for zero phase-sequence longitudinal protection.

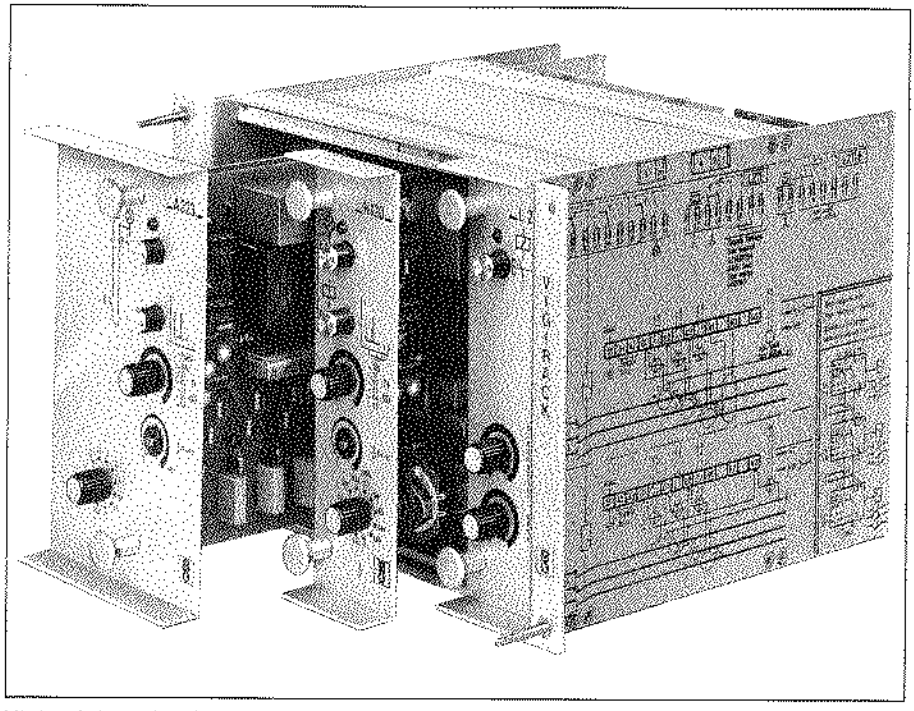
With an overcurrent PCB alone or grouped with a zero phase-sequence PCB
which can receive a logic wait signal but cannot send one out and will in most cases be placed at the head of the installation.

With overcurrent, zero phase-sequence and logic PCB'S
which provide protection against overcurrents (short-circuits) earth faults and carry out logic selectivity.

Some interesting characteristics
- testing: possibility of testing for a phase or an earth fault with and without sending of a trip signal;
- differentiated signalling for phase and earth faults with memorizing;
- supply source which can be different for the Logic wait function and for the relay itself because of the galvanic isolation between the two racks (linked functionally by the "logic" wire, often called "pilot" wire). This characteristic gives great flexibility in use;
- outputs:
with time-lag (T_1): two reversing contacts available;
instantaneous: one working contact available.
- inputs: zero impedance for inputs connected to the CT's;
anti-harmonic filters;
a supplementary input point, making it possible to take into account logically any "fault" data sent by another protecting relay;
- taking into account of any zero-sequence fault data on the common phase of the 3 CT's or by rings;
- "pilot wire": if in a single unit the CAHL relays are supplied by the same auxiliary source, it is possible for the pilot wire to have only a single conductor instead of two.



Vigirack type 4, front view


Vigirack type 4, relay draws in "out" position

use of the logic selectivity protection

The logic selectivity protection can be employed on distribution networks of any structure and both for high voltages and the main low-voltage outputs.

Antenna type networks
The explanations given in the paragraph entitled "Principle of logic selectivity (SSL)" correspond to this type of network.

Open loop networks
According to the position of the breaking point, the signals emitted by the Vigirack relays associated to the loop circuit-breakers must be oriented towards one or other of the arrival points.
This orientation can be obtained either by the use of single-phase current, directional relays or by employing the auxiliary contacts of the loop circuit-breakers (see Figure 6).

Close-loop networks
The time-lag signals must be correctly oriented by directional power relays according to the direction of flow of the energy during the fault. If the protected network has not an isolated neutral, it is necessary to use either zero phase-sequence directional relays or zero phase-sequence longitudinal protections.

Network operating in "open loops".

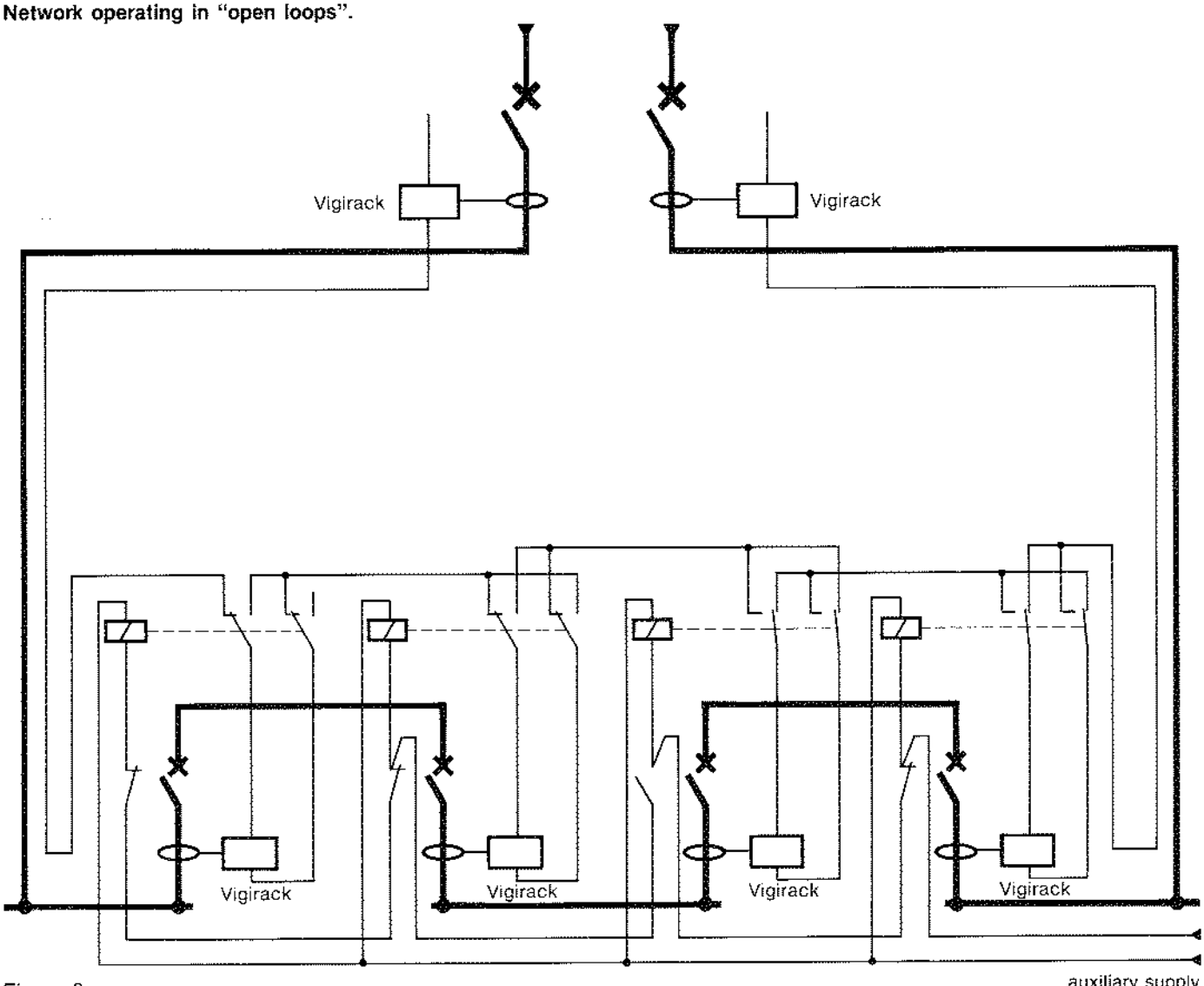


Figure 6

advantages of a logic selectivity protection

Apart from the selectivity of the protection, which is the primary characteristic of the system, the speed of tripping makes it possible to reduce the specifications relating to the behaviour of the conductors of the equipment and the current transformers, under short-circuit conditions, to values which represent an appreciable saving.
The system is very reliable; as we have seen, it consists in the possibility of the down-stream relay increasing intelligently the up-stream relay's own time-lag. Under no circumstances can a fault affect all the protections. The system makes use of course of a time-lag selectivity and presents the big advantage of making it possible to obtain non-cumulative tripping times.
The system provides a solution to the problem of the selectivity at tripping for a whole network, right from the main low-voltage feeders points to the high voltage feeders.
There is only one restriction: the need to have a pilot-wire connection between the various stages of the protection; this is a minor disadvantage compared to all the advantages which the system provides.
The setting-up of this protective system is fairly simple; it can be applied to both experimental and existing installations, and allows extensions to be made without modifying the circuit values.
Furthermore, since the system is independent of the number of stages protected, the design of the networks can be based on the real needs of the user, and not on the demands of the distributor.

bibliography:

(1) La sélectivité des protections.
F. Sautriau, Cahiers Techniques MG, n° 13.
(2) Brevet français n° 1 421 236.
(3) Leaflet on Vigirack protection systems E/F 11,015 a.

Roland Calvas
Engineer, graduated from ENSERG in 1964 and later from the I.A.E. He started working for MG in 66. He was first in charge of teaching electronics both within MG and outside as part of a university-industry relations programme.
After having worked in the field of static convertors he became a sales manager then products' manager for the personnel and electric machine protection relay activity. During this period he participated in the development of the "Logic selectivity" technique. He is now quality manager of MG's Terminal Distribution Division.

François Sautriau
Engineer, graduated from the "Ecole Supérieure d'Electricité" in 1968. He came to Merlin Gerin in March 1970. He was systems designer in the contracting department up to 1976 then chief project engineer in the technical branch of DRE (Contracting Department). He is at present head of the industrial projects group in DRE's technical branch.

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